

UDAYA PRIYA S

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PROFESSIONAL SUMMARY

M.Tech student in Digital Communication Engineering (graduating 2026) with hands-on experience in embedded software development, digital signal processing, and hardware/software debugging. Proficient in C, C++, and Python, with practical exposure to embedded systems programming (Arduino, Embedded C), FPGA-based digital design (Verilog, Xilinx Vivado), and circuit simulation (Cadence Virtuoso, ANSYS HFSS). Experienced in structured development processes, unit testing, and debugging using development and simulation tools. Seeking an internship or entry-level role in Digital Signal Processing (DSP) or Embedded Software Development to apply this foundation in a real-time, hardware-adjacent development environment.

TECHNICAL SKILLS

Domain Knowledge: Digital Signal Processing (DSP), Embedded Systems, Digital Communication Systems, Underwater Optical Communication, FPGA Development, Analog and Digital Circuits, VLSI Design Flow (RTL to GDS)

Programming Languages: C, Embedded C, Python, MATLAB, Verilog RTL, SystemVerilog

Tools and Software: Xilinx Vivado, Cadence Virtuoso, Cadence Innovus, ANSYS HFSS, Visual Studio Code, Arduino IDE

Techniques: Artificial Neural Networks (ANN), Adaptive Modulation

Testing and Debugging: Unit-level testing and simulation debugging (FPGA/RTL simulation), circuit-level simulation and validation (Cadence), version-controlled iterative development

Professional Skills: Problem Solving, Analytical Thinking, Team Collaboration, Quick Learner

EDUCATION

M.Tech, Digital Communication Engineering — BMS College of Engineering, Bengaluru 2024 - 2026
CGPA: 8.24

B.E., Electronics and Communication Engineering — SJC Institute of Technology, Chikkaballapur 2020 - 2024
CGPA: 7.82

Class XII (PCMB) — Varadadri PU College, Bagepalli 2018 - 2020
Percentage: 81.33%

Class X — Young India High School, Bagepalli 2009 - 2018
Percentage: 89.28%

WORK EXPERIENCE

Assistant Professor, Department of Computer Science and Engineering (CSE) — SJC Institute of Technology, Chikkaballapur Sep 2026 - Present

Intern, VLSI and Semiconductor — Chips-to-Startup (C2S) Program, BMSCE Sep 2025 - Jan 2026

- Gained hands-on experience in the **RTL-to-GDSII VLSI design flow**, understanding the complete digital IC design process.
- Developed digital design and verification skills using **Verilog** and **System Verilog**, with exposure to RTL design, synthesis, and implementation.
- Acquired practical knowledge of **Physical Design (PD)**, including floor planning, placement, clock tree synthesis (CTS), routing, timing analysis, and physical verification.
- Worked with **Cadence Virtuoso** to understand custom IC design concepts and industry-standard semiconductor design workflows.
- Strengthened understanding of semiconductor design methodologies, EDA tools, and digital IC design while enhancing analytical, problem-solving, and teamwork skills.

Intern, Telecommunication Department — BSNL (Bharat Sanchar Nigam Limited) Sep 2023 - Nov 2023

- Gained hands-on exposure to **telecommunication networks** and communication systems through industrial training at Bharat Sanchar Nigam Limited.
- Learned the architecture and operation of **Optical Fiber Communication (OFC)**, **GSM/mobile networks**, broadband services, and switching systems.
- Observed the installation, configuration, and maintenance of telecom equipment and network infrastructure.
- Understood the fundamentals of **signal transmission**, network management, and communication protocols.
- Acquired practical knowledge of telecom operations, fault diagnosis, and troubleshooting techniques in a real-world environment.

CERTIFICATIONS

- RTL to GDS II - Training Programme, Latch Q Semiconductor Pvt. Ltd. (under C2S)
- VLSI Design Flow: RTL to GDS, NPTEL, India.
- Microelectronics: Device to Circuit, VTU, India.
- Fundamentals of Micro and Nano Fabrication, VTU, India.
- Research Methodology and IPR, VTU, India.

PROJECTS

AI-Enabled Adaptive Multi-User Underwater Optical Communication System

Jan 2026 - Jun 2026

- Designed and simulated an AI-enabled, multi-user Underwater Wireless Optical Communication (UWOC) system combining Optical Code Division Multiple Access (OCDMA) with OOK, PPM, and OFDM modulation schemes.
- Developed an Artificial Neural Network (ANN)-based adaptive modulation-selection module that dynamically selects the optimal modulation scheme in real time based on channel conditions (SNR, BER, attenuation, transmission distance).
- Modelled realistic underwater channel impairments (absorption, scattering, turbulence) and evaluated system performance in MATLAB across BER, SNR, throughput, and spectral efficiency metrics.
- Co-authored an IEEE paper presenting the proposed AI-assisted adaptive modulation framework for robust, real-time underwater optical communication.
- **Tools:** MATLAB

TMR Architecture for Fast FIR Algorithm

Jan 2025 - Feb 2025

- Designed a fault-tolerant FIR filter using Triple Modular Redundancy (TMR) with a three-parallel Fast FIR architecture, applying core digital signal processing concepts.
- Implemented and evaluated RTL design on FPGA, performing simulation-based debugging and unit-level verification of filter performance, power, and resource efficiency.
- **Tools:** Xilinx Vivado, Verilog

Monitoring Study Habits using Arduino

Apr 2023 - Jun 2023

- Developed Embedded C firmware on Arduino for a real-time IoT-based monitoring system tracking study, rest, and distraction time patterns via Arduino Cloud.
- Performed hands-on hardware debugging and iterative testing to validate sensor data accuracy and system reliability.

Machine Learning Approach to Personalize Study Habit Analysis

Nov 2023 - Mar 2024

- Built a focus-monitoring system using facial expression recognition with Python and OpenCV/ML libraries in Visual Studio Code.
- Wrote and debugged Python scripts for data processing and model integration, including unit-level testing of individual modules.

Performance Enhancement of 6T SRAM using Stacked SRAM

Sep 2025 - Jan 2026

- Enhanced conventional 6T SRAM using stacked transistor architecture to reduce leakage current and improve read Static Noise Margin (SNM).
- Conducted circuit-level simulations to validate read/write performance; achieved better area-power efficiency for low-power applications.
- **Tools:** Cadence Virtuoso

Design of Vivaldi Antenna

May 2025 - Jul 2025

- Designed a wideband Vivaldi antenna for high-frequency applications using ANSYS HFSS.
- Performed electromagnetic simulations for radiation patterns, return loss, and impedance matching; prepared layout for fabrication.
- **Tools:** ANSYS HFSS

Design of 180-Degree Ring Coupler

May 2025 - Jul 2025

- Designed and simulated a 180-degree ring coupler for RF and microwave applications using ANSYS HFSS.
- Applied S-parameter analysis and transmission line theory; optimized for isolation, return loss, and phase balance.
- **Tools:** ANSYS HFSS

EXTRACURRICULAR ACTIVITIES

- Member of College NCC Team; contributed to social service activities.
- Participated in SEED (Social Entrepreneurship and Empowerment for Development) activities.
- Worked as Placement Coordinator, facilitating student placements in the final year.
- Attended technical workshop by Aqmenz Automation Pvt. Ltd. on Python Coding with Application Projects, Feb 2022.
- Led stage and decoration management for the college farewell event.